## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s):

Fong PONG

Confirmation No.:

**Application No.:**09/444,173

**Examiner:** Jasmine Song

Filing Date:

11/19/99

Group Art Unit: 2187

Title:

ASYNCRONOUS CACHE COHERENCE ARCHITECTURE IN A SHARED MEMORY

MULTIPROCESSOR WITH POINT-TO-POINT LINKS

RECEIVED

DEC 1 2 2001

COMMISSIONER FOR PATENTS Washington, D.C. 20231

Technology Center 2100

	TRANSMITTAL LETTER FOR RESPONSE/AMENDMENT
Sir:	

(X) ( ) (X)	Respons	se/Amendment e as calculated below	v	n the above-identified ( ( e to "Box Non-Fee Ar	) Petition	on to extend emental Dec	time to respond laration
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	(1) FOR	(2) CLAIMS REMAINING AFTER AMENDMENT	(3) NUMBER EXTRA	(4) HIGHEST NUMBER PREVIOUSLY PAID FOR	(5) PRESENT EXTRA	(6) RATE	(7) ADDITIONAL FEES
	TOTAL					<del>                                     </del>	-

FEES		HATE		EXTRA		SLY PAID FOR		EXTRA	TER AMENDMENT		
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0	\$	1 MONTH 440.00				MONTH 3RD MONTH 0.00 \$920.00			1ST MONTH \$110.00	ON	EXTENSION FEE
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0	\$	TOTAL ADDITIONAL FEE FOR THIS AMENDMENT									

to Deposit Account 08-2025. At any time during the pendency of this application, please charge any fees required or credit any overpayment to Deposit Account 08-2025 pursuant to 37 CFR 1.25. Additionally please charge any fees to Deposit Account 08-2025 under 37 CFR 1.16 through 1.21 inclusive, and any other sections in Title 37 of the Code of Federal Regulations that may regulate fees. A duplicate copy of this sheet is enclosed.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231.

Date of Deposit:

Typed Name:

Signature:

Respectfully submitted,

Fong PONG

John W. Ryan

Attorney/Agent for Applicant(s)

Reg. No. 33,771

Date: December 10, 3001

Telephone No.: (202) 663-6446

Applicant's Docket No. 10981470-1



PATENT 13/07

## <u>IN THE UNITED STATES PATENT AND TRADEMARK OFFICE</u>

RECEIVED

Applicant:

Fong PONG

DEC 1 2 2001

**Technology Center 2100** 

U.S. Serial No.:

09/444,173

Art Unit:

2187

Filed:

November 19, 1999

Examiner:

Jasmine Song

For:

ASYNCHRONOUS CACHE COHERENCE ARCHITECTURE IN A SHARED MEMORY MULTIPROCESSOR WITH POINT-TO-POINT

LINKS

Box AF

**Assistant Commissioner of Patents** 

Washington, D.C. 20231

enter

## RESPONSE TO FINAL OFFICE ACTION UNDER 37 CFR § 1.116

In response to the Final Office Action mailed October 10, 2001, Applicant respectfully requests the Examiner to enter the following amendments and consider the following remarks:

## IN THE SPECIFICATION:

On page 7, please substitute the paragraph starting on line 8 with the paragraph below:

Preferably, the request queues communicate requests via a high-speed internal address bus or switch 223 (referred to generally as a "bus" or "control path interconnect"). Each of the processors and main memory devices are capable of storing a copy of a requested data block. Therefore, each has a corresponding destination buffer (e.g., queues 224, 226, 228, 230) in the memory controller for receiving memory requests